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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) SON-3173	
	Application Number 10/584,994-Conf. #5930	Filed June 29, 2006
	First Named Inventor Masaaki Bairo	
	Art Unit 2826	Examiner W. W. Kuo

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 40,290
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

40,290
Signature

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Typed or printed name

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Telephone number

May 22, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[x] *Total of 1 forms are submitted.

Docket No.: SON-3173
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaaki Bairo

Application No.: 10/584,994 Confirmation No.: 5930

Filed: June 29, 2006 Art Unit: 2826

For: BIPOLAR TRANSISTOR, SEMICONDUCTOR APPARATUS HAVING THE BIPOLAR TRANSISTOR, AND METHODS FOR MANUFACTURING THEM Examiner: W. W. Kuo

REQUEST FOR PRE-APPEAL BRIEF PANEL REVIEW OF REJECTION

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Final Office Action of February 22, 2008.

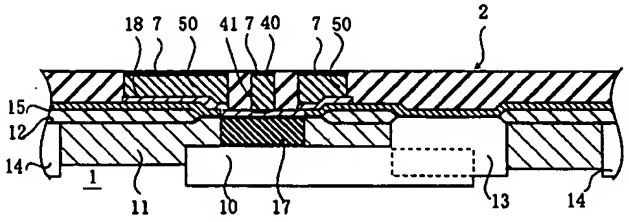
Regarding claims 9-13 and 15 - The cancellation of claims 9-13 and 15 has been proposed within the After Final Amendment of March 13, 2008.

Claim 14 - The placement of claim 14 into independent form has been proposed within the After Final Amendment of March 13, 2008.

Claim 14 is drawn to a method for manufacturing a bipolar transistor that includes the step of depositing a silicide (7) onto a polished surface of said conducting film (40, 50).

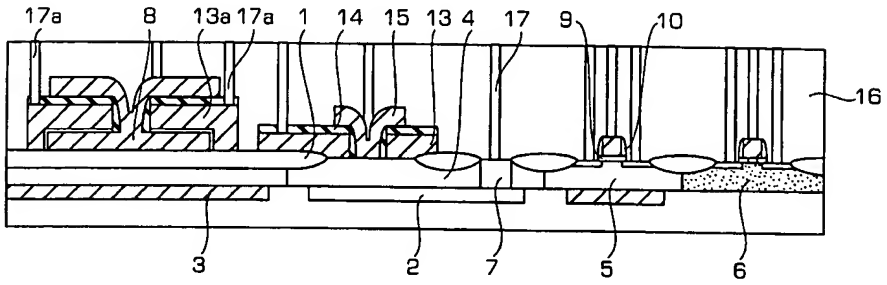
Figure 7 of the specification as originally filed is provided hereinbelow.

FIG. 7



Fujii - Figure 9 of Fujii is provided hereinbelow.

FIG. 9



Fujii arguably discloses the presence of a base electrode 13 and an emitter electrode 15 (Fujii at column 4, lines 37 and 39). Fujii, at column 8, lines 27-30, provides that after this, as shown in FIG. 9, a *first interlayer insulating film 16* is formed over the entire surface, and *holes are made at required positions* and *filled up with polysilicon*, and thereby *first layer contacts 17* are formed.

However, the Office Action readily admits that Fujii fails to teach the holes being simultaneously formed (Office Action at page 4).

- ***Thus, Fujii fails to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening.***

Whereas Fujii arguably discloses that *holes are made at required positions* and *filled up with polysilicon* (Fujii at 8, lines 28-29), the Office Action ***readily admits*** that Fujii ***fails*** to disclose, teach or suggest *polishing* the polysilicon to separate the contacts 17.

- ***Thus, Fujii fails to disclose, teach, or suggest polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

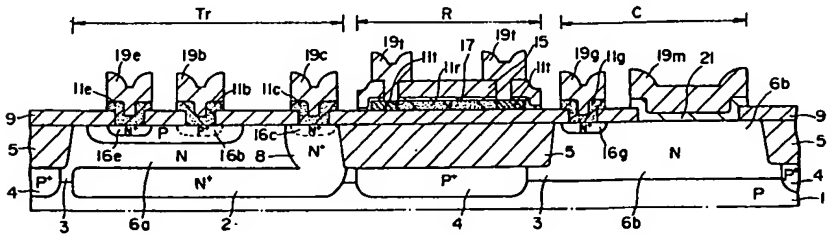
Fujii arguably discloses that in the first and the second embodiments described above, the first electrode of the ***capacitor*** and the ***gate electrodes*** of the MOSFETs are formed of polysilicon. However, the use of polycide that is *silicided* polysilicon with titanium, cobalt, molybdenum, tungsten or the like, is preferable, since it reduces the resistance value of the capacitor further down.

However, Fujii ***fails*** to teach a silicided base electrode lead portion or a silicided emitter electrode lead portion.

- ***Thus, Fujii fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Hozumi - Figure 2M of Hozumi is provided hereinbelow.

FIG. 2M



Hozumi arguably discloses the presence of a base region 7.

However, the Office Action fails to show wherein there is to be found within Hozumi a step of forming the base region 7 on an insulator.

- ***Thus, the Office Action fails to show within Hozumi a step of forming a base layer on an insulator, said base layer being in contact with a portion of a semiconductor substrate.***
- ***Moreover, the Office Action fails to show that Hozumi teaches polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

In addition, the Office Action fails to show wherein there is to be found within Hozumi a silicided base electrode lead portion or a silicided emitter electrode lead portion.

- ***Thus, the Office Action fails to show that Hozumi teaches depositing a silicide onto a polished surface of said conducting film.***

Morimoto - Morimoto arguably discloses that then, *surface polishing by the CMP method* is performed starting with the surface of the tungsten film 14 to *remove the tungsten and titanium nitride films* other than the film portions filled in the via holes, whereby a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13, as shown in FIG. 2C (Morimoto at column 6, lines 18-24).

Figures 2B-2C of Morimoto are provided hereinbelow.

Fig. 2B

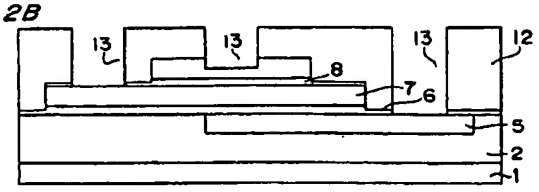
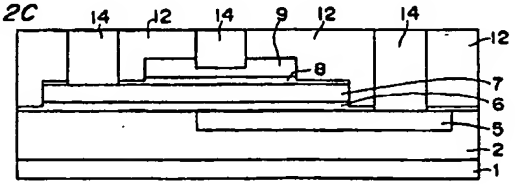


Fig. 2C



Whereas the figures of Morimoto depict a capacitor, Morimoto ***fails*** to teach the presence of a bipolar transistor. Additionally, Morimoto arguably discloses a tungsten plug 14 (Morimoto at column 6, line 19). However, Morimoto ***fails*** to teach a *silicided* plug 14.

- ***Thus, Morimoto fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Besser - Figure 1 of Besser is provided hereinbelow.

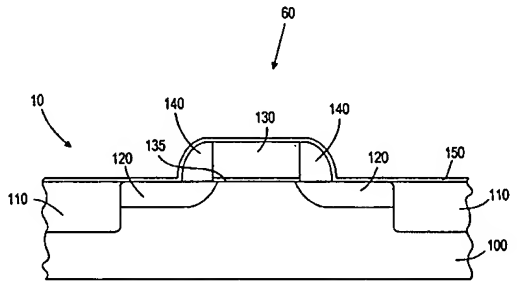


Fig. 1

Besser ***fails*** to disclose, teach, or suggest gate region 130 as being polished.

- ***Thus, Besser fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Dated: May 22, 2008

Respectfully submitted,

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